	Type	L #	Hits	Search Text	DBs
1	BRS	L1	2	"6436768".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L2	0	(pattern$3 near3 wordline$1) near15 (bitline41)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L3	41	(pattern$3 near3 wordline$1) near15 (bitline$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L4	314	(wordline$1) near15 (bitline$1) near15 (insulat$3 or dielectric)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
5	BRS	L5	23	(wordline$1) near15 (bitline$1) near15 (insulat$3 or dielectric) near15 (charge near trapping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
6	BRS	L6	508631	(pocket neat implant$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
7	BRS	L7	123	(pocket neat implant$3) near25 (charge near trapping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
8	BRS	L8	125	(pocket neat implant$3) near45 (charge near trapping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
9	BRS	L9	0	(pocket near implant$3) near45 (charge near trapping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
10	BRS	L10	0	(pocket near5 implant$3) near45 (charge near trapping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
11	BRS	L11	0	(pocket near5 implant$3) near45 (charge near5 trapping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
12	BRS	L12	24	(pocket near5 implant$3) near45 (charge or trapping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
13	BRS	L13	16	(pocket near implant$3) near45 (charge or trapping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
14	BRS	L14	4	(pocket near implant$3) near45 (bitline$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
15	BRS	L15	30	(pocket near implant$3) near45 (bit near line$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	U	1	Document ID	Title
1			US 20030205747 A1	Self-aligned source pocket for flash memory cells
2			US 20030082839 A1	Method for calculating threshold voltage of pocket implant mosfet
3			US 20020187617 A1	Self-aligned source pocket for flash memory cells
4			US 20020106866 A1	Self-aligned source pocket for flash memory cells
5			US 6864523 B2	Self-aligned source pocket for flash memory cells
6			US 6806143 B2	Self-aligned source pocket for flash memory cells
7			US 6800891 B2	Self-aligned source pocket for flash memory cells
8			US 6429063 B1	NROM cell with generally decoupled primary and secondary injection
9			US 6103602 A	Method and system for providing a drain side pocket implant

	U	1	Document ID	Title
10			US 5926712 A	Process for fabricating MOS device having short channel
11			US 5793070 A	Reduction of trapping effects in charge transfer devices
12			US 5786620 A	Fermi-threshold field effect transistors including source/drain pocket implants and methods of fabricating same
13			US 5321283 A	High frequency JFET
14			US 4683485 A	Technique for increasing gate-drain breakdown voltage of ion-implanted JFET

	U	1	Document ID	Title
15			US 20030205747 A	Forming self-aligned source pockets in flash memory cells involves implanting dopant into substrate through respective substrate regions to form dopant pockets beneath source regions
16	X		US 5926712 A	Production of metal oxide semiconductor (MOS) device having short channel